What is claimed is:

1. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material that includes a memory area and a peripheral area;

a memory cell formed in the memory area of the substrate, wherein the memory cell includes:

an electrically conductive floating gate disposed over and insulated from the substrate,

an electrically conductive control gate disposed adjacent to the floating gate, and

an insulating layer formed in the memory and peripheral areas that includes a first portion that is disposed between the control gate and the floating gate with a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an MOS transistor formed in the peripheral area of the substrate, wherein the MOS transistor includes:

an electrically conductive poly gate disposed over and insulated from the substrate, and

a second portion of the insulating layer being disposed between the poly gate and the substrate and having a thickness that is greater than that of the first portion of the insulating layer;

wherein the first and second portions of the insulating layer being initially formed as a continuous layer of material.

2. The device of claim 1, wherein the memory cell further includes:

a first source region and a first drain region formed in the substrate, with a first channel region therebetween, wherein the floating gate is disposed over and insulated from at least a portion of the first channel region.

3. The device of claim 2, wherein the MOS transistor further includes:

a second source region and a second drain region formed in the substrate, with a second channel region therebetween, wherein the poly gate is disposed over and insulated from at least a portion of the second channel region.

4. The device of claim 1, wherein the control gate has a first portion that is disposed laterally adjacent to the floating gate.

5. The device of claim 4, wherein the control gate first portion is disposed over a portion of the first channel region.

6. The device of claim 5, wherein the control gate has a second portion that is disposed over the floating gate.

7. The device of claim 1, wherein:

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.

8. The device of claim 7, wherein the insulating layer first portion further extends between the substrate and the control gate.

9. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material that includes a memory area and a peripheral area;

a memory cell formed in the memory area of the substrate, wherein the memory cell includes:

a first source region and a first drain region formed in the substrate, with a first channel region therebetween,

an electrically conductive floating gate disposed over and insulated from at least a portion of the first channel region,

an electrically conductive control gate disposed adjacent to the floating gate, and

an insulating layer formed in the memory and peripheral areas, wherein the insulating layer has a first portion that is disposed between the control gate and the floating gate with a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an MOS transistor formed in the peripheral area of the substrate, wherein the MOS transistor includes:

a second source region and a second drain region formed in the substrate, with a second channel region therebetween,

an electrically conductive poly gate disposed over and insulated from at least a portion of the second channel region, and

a second portion of the insulating layer being disposed between the poly gate and the second channel region, wherein the second portion of the insulating layer has a thickness that is greater than that of the first portion of the insulating layer;

wherein the first and second portions of the insulating layer being initially formed as a continuous layer of material.

10. The device of claim 9, wherein the control gate has a first portion that is disposed laterally adjacent to the floating gate.

11. The device of claim 10, wherein the control gate first portion is disposed over a portion of the first channel region.

12. The device of claim 11, wherein the control gate has a second portion that is disposed over the floating gate.

13. The device of claim 9, wherein:

the insulating layer second portion is formed directly over the peripheral area of the substrate, and the poly gate is formed directly over the insulating layer second portion.

14. The device of claim 13, wherein the insulating layer first portion further extends between the substrate and the control gate.

15. A method of making an electrically programmable and erasable memory device, comprising the steps of:

forming an electrically conductive floating gate disposed over and insulated from a memory area of a substrate;

forming an insulating layer that has a first portion formed over the memory area of the substrate and a second portion formed over a peripheral area of the substrate, wherein the insulating layer first portion has a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

changing a thickness of one of the insulating layer first and second portions relative to the other of the insulating layer first and second portions;

forming an electrically conductive control gate disposed adjacent to the floating gate and insulated therefrom by the first portion of the insulating layer; and

forming an electrically conductive poly gate disposed over the peripheral area of the substrate and insulated therefrom by the second portion of the insulating layer.

16. The method of claim 15, further comprising the steps of:

forming a first source region and a first drain region in the substrate, with a first channel region therebetween, wherein the floating gate is disposed over and insulated from at least a portion of the first channel region; and

forming a second source region and a second drain region in the substrate, with a second channel region therebetween, wherein the poly gate is disposed over and insulated from at least a portion of the second channel region.

17. The method of claim 15, wherein the formation of the control gate and the poly gate includes the steps of:

depositing a layer of conductive material over the insulating layer; and

selectively removing portions of deposited conductive material except for a first portion thereof forming the control gate and a second portion thereof forming the poly gate.

18. The method of claim 15, wherein the changing of the relative thickness of the insulating layer first and second portions includes the steps of:

forming a layer of material over the insulating layer;

masking a first portion of the layer of material formed over the first portion of the insulating layer, wherein a second portion of the layer of material formed over the second portion of the insulating layer is left unmasked;

removing the unmasked second portion of the layer of material to expose the second portion of the insulating layer; and

increasing the thickness of the exposed second portion of the insulating layer.

19. The method of claim 18 wherein the increasing of the thickness of the exposed insulating layer second portion includes thermally oxidizing the exposed insulating layer second portion.

20. The method of claim 15, wherein the changing of the relative thickness of the insulating layer first and second portions includes the steps of:

forming a layer of material over the insulating layer;

masking a first portion of the layer of material formed over the second portion of the insulating layer, wherein a second portion of the layer of material formed over the first portion of the insulating layer is left unmasked;

removing the unmasked second portion of the layer of material to expose the first portion of the insulating layer; and

removing a top portion of the exposed first portion of the insulating layer.

21. A method of forming an electrically programmable and erasable memory device, comprising the steps of:

forming a memory cell in a memory area of a substrate, wherein the memory cell formation includes the steps of:

forming a floating gate over and insulated from the substrate, and

forming a control gate adjacent to and insulated from the floating gate;

forming an MOS transistor in a peripheral area of the substrate, wherein the MOS transistor formation includes forming a poly gate over and insulated from the substrate;

wherein the formation of the memory cell and the formation of the MOS transistor together include the step of:

forming an insulating layer having a first portion that is disposed between the control gate and the floating gate with a thickness permitting Fowler-Nordheim tunneling of charges therethrough, and a second portion that is disposed between the poly gate and the substrate, wherein the second portion of the insulating layer has a thickness that is greater than that of the first portion of the insulating layer.

22. The method of claim 21, further comprising the steps of:

forming first source and drain regions with a first channel region therebetween in the substrate, wherein the floating gate is disposed over at least a portion of the first channel region; and

forming second source and drain regions with a second channel region therebetween in the substrate, wherein the poly gate is disposed over at least a portion of the second channel region.

23. The method of claim 21, wherein the formation of the insulating layer includes the steps of:

forming the first and second portions of the insulating layer with a uniform thickness over the memory and peripheral areas of the substrate; and

changing the thickness of one of the insulating layer first and second portions relative to the thickness of the other of the insulating layer first and second portion.

24. The method of claim 21, wherein the formation of the control gate and the poly gate includes the steps of:

depositing a layer of conductive material over the insulating layer; and

selectively removing portions of deposited conductive material except for a first portion thereof forming the control gate and a second portion thereof forming the poly gate.

25. The method of claim 23, wherein the changing of the relative thickness of the insulating layer first and second portions includes the steps of:

forming a layer of material over the insulating layer;

masking a first portion of the layer of material formed over the insulating layer first portion, wherein a second portion of the layer of material formed over the second portion of the insulating layer is left unmasked;

removing the unmasked second portion of the layer of material to expose the insulating layer second portion; and

increasing the thickness of the exposed second portion of the insulating layer.

26. The method of claim 25 wherein the increasing of the thickness of the exposed insulating layer second portion includes thermally oxidizing the exposed insulating layer second portion.

27. The method of claim 23, wherein the changing of the relative thickness of the insulating layer first and second portions includes the steps of:

forming a layer of material over the insulating layer;

masking a first portion of the layer of material formed over the second portion of the insulating layer, wherein a second portion of the layer of material formed over the first portion of the insulating layer is left unmasked;

removing the unmasked second portion of the layer of material to expose the first portion of the insulating layer; and

removing a top portion of the exposed first portion of the insulating layer.